

FIG. 1

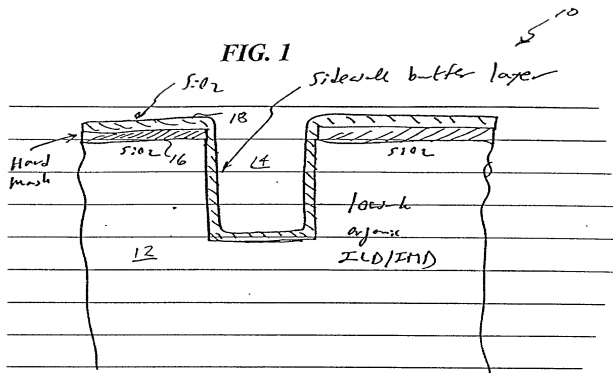
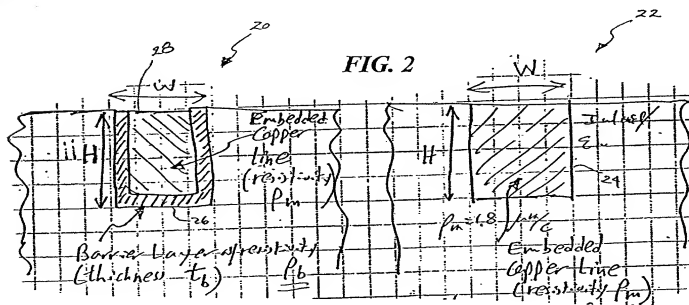


FIG. 2



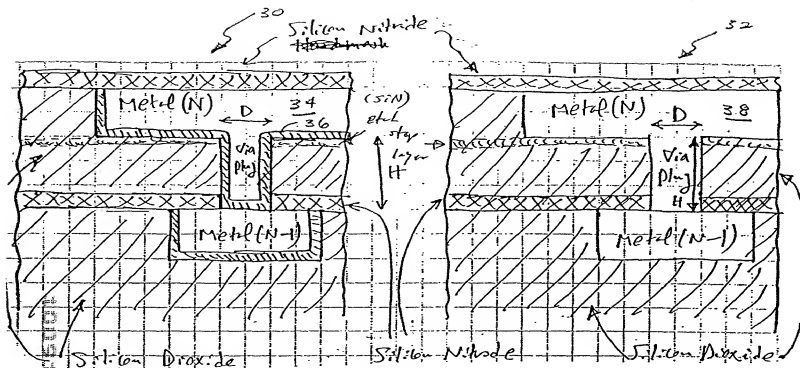


FIG. 3

FIG. 4

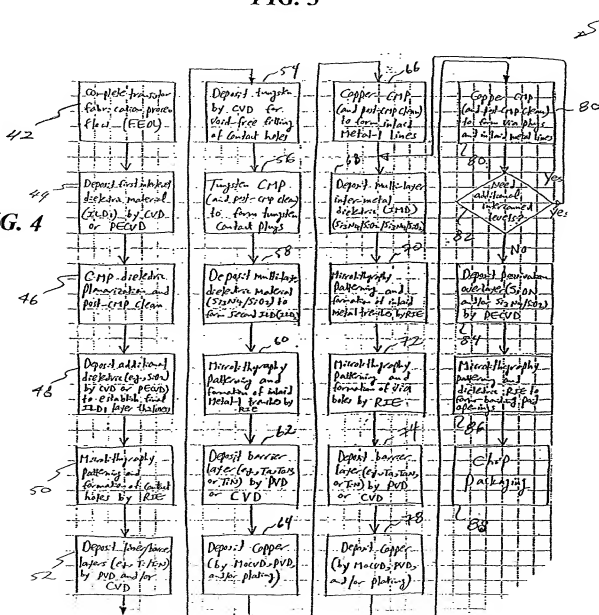


FIG. 5

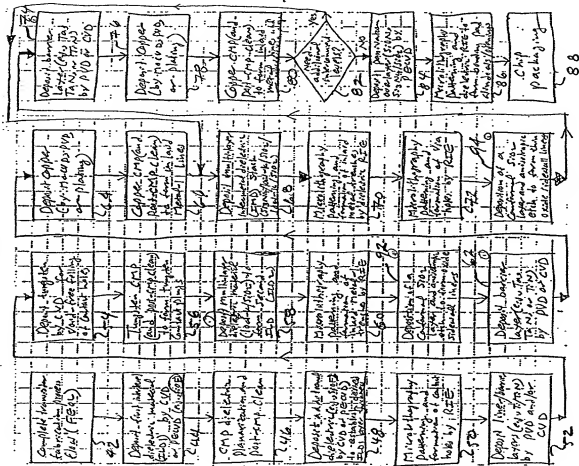
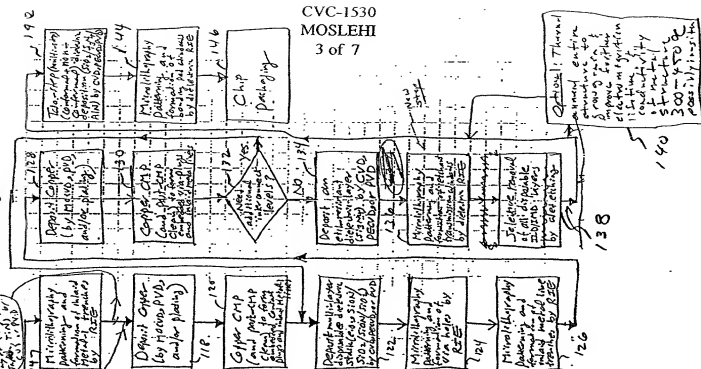


FIG. 6



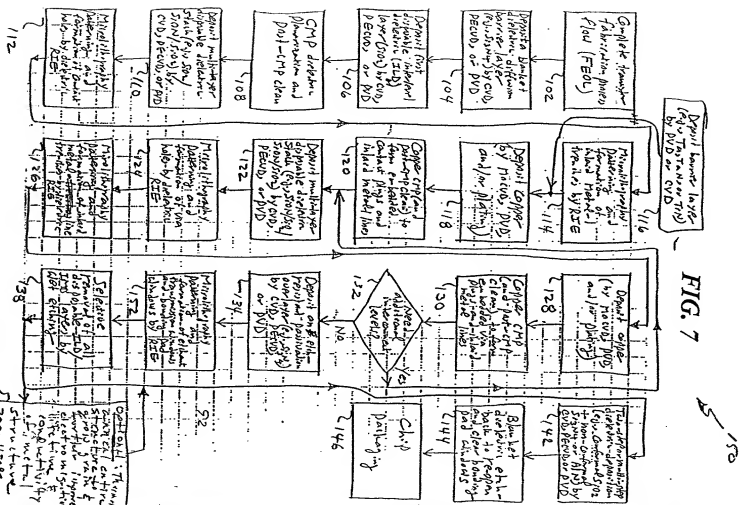


FIG. 8 Top Layer of Etch-Resistant Dielectric (Silicon Nitride or Aluminum Nitride)

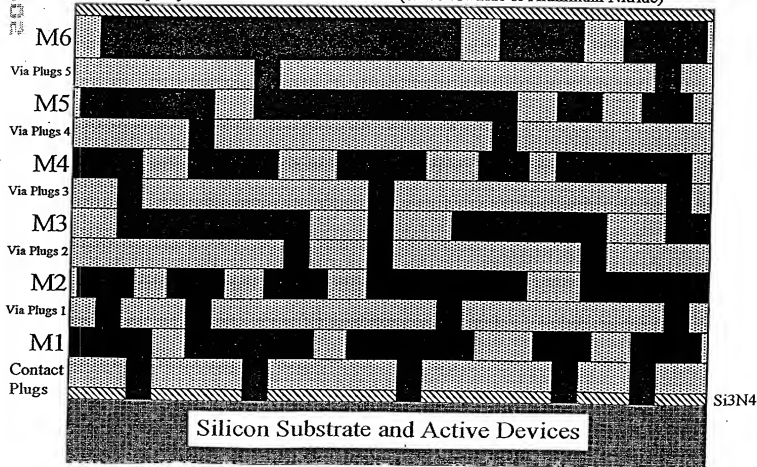


FIG. 10

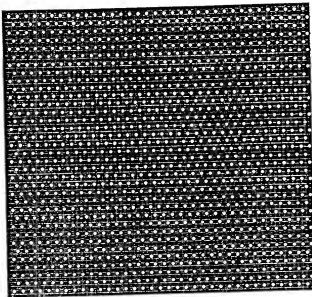


FIG. 9

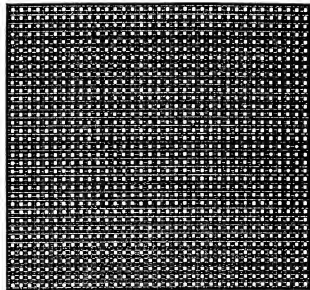


FIG. 12

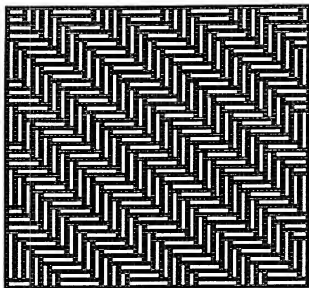
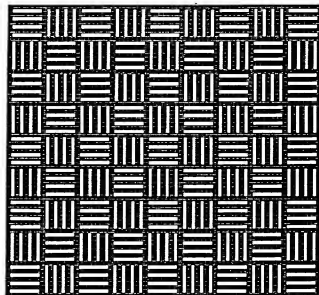


FIG. 11



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FIG. 13

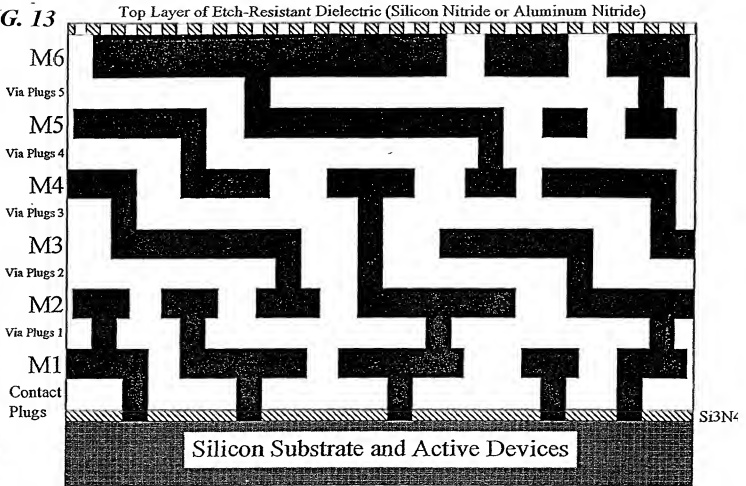
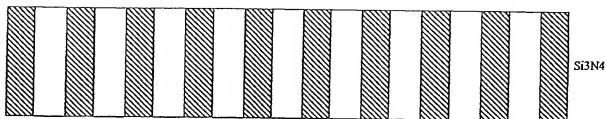


FIG. 14

Top dielectric layer (e.g., Si3N4) with etchant transmission windows (e.g., minimum geometry holes)



Hermetic Sealing Process

After conformal deposition of first dielectric (e.g., CVD SiO2 or Si3N4 or AlN) followed by non-conformal deposition of second sealing dielectric (e.g., PVD of AlN or DLC or Si3N4)

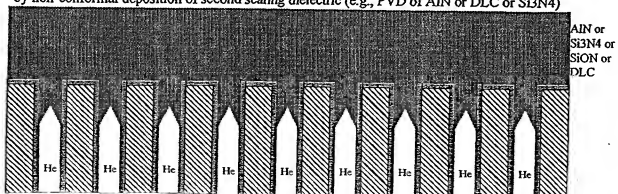


FIG. 15

